STANDARD LOGIC SYSTEM – DIRECTIONS FOR USE

1. GENERAL

   a) THE STANDARD LOGIC SYSTEM CONSISTS OF THE STANDARD LOGIC MODULES LISTED ON THIS DRAWING

   b) THESE LOGIC MODULES ARE DESIGNED TO BE ABLE TO BE INTERCONNECTED WITH SOFTWARE LOGIC LINKS SO AS TO PROVIDE COMPLETE CONTROL LOGIC SYSTEMS

2. DESIGN SUMMARY LOGIC DRAWINGS

   DESIGN SUMMARY LOGIC DRAWINGS SHALL CONSIST OF THE PROJECT SPECIFIC LOGIC MODULE INTERCONNECTION DIAGRAMS SHOWING:

   a) ON EACH STANDARD MODULE BLOCK, THE ASSOCIATED FS00–2 DRAWING NUMBER AND REVISION IDENTIFIER AS WELL AS THE NAMES OF THE INPUT AND OUTPUT BUSES TO BE USED

   b) ON EACH SPECIAL LOGIC MODULE, THE RELEVANT INPUT AND OUTPUT BUSES, AND

   c) A DESCRIPTION OF THE LOGIC TO BE EXECUTED IN EACH SPECIAL LOGIC MODULE IN ACCORDANCE WITH NOTE 5 HEREUNDER

3. PROJECT LOGIC MODULE INTERCONNECTION DIAGRAMS

   a) PROJECT MODULE INTERCONNECTION DIAGRAMS SHALL SHOW THE INTERCONNECTING LOGIC LINKS BETWEEN ALL STANDARD MODULES AND SPECIAL MODULES TO BE USED IN THE PROJECT CONTROL LOGIC, SIMILAR TO THE EXAMPLES SHOWN IN THE FS00–3 SERIES OF DRAWINGS

   b) LOGIC MODULE INPUTS AND OUTPUTS WHICH ARE NOT TO BE USED IN PARTICULAR APPLICATIONS SHALL NOT BE SHOWN ON PROJECT SPECIFIC DESIGN SUMMARY MODULE INTERCONNECTION DIAGRAMS

   c) FROM TIME TO TIME IT WILL BE NECESSARY TO ASSIGN AN INPUT OR OUTPUT, WITHIN A STANDARD MODULE, A FUNCTION NAME DIFFERENT FROM THE NAME SPECIFIED ON THE STANDARD MODULE DRAWING.
   IN SUCH CASES, THE PROJECT MODULE INTERCONNECTION DIAGRAMS SHALL SHOW THE STANDARD MODULE I/O NAME IN PARENTHESES NEXT TO THE ASSOCIATED PROJECT LOGIC BUS NAME, e.g. UNIT 1 LEAKAGE FAULT (UNIT 1 SUNDRY FAULT)

   d) THE PROJECT DESIGNER MAY CHOOSE TO INDICATE THE CONDITION OF ANY INTERCONNECTING LOGIC BUS AT THE LOCAL UNIT DISPLAYS, THE LOCAL COMMON DISPLAY AND/OR SCADA. FS00–2 SERIES OF DRAWINGS SHOWS WHICH LOGIC BUS CONDITIONS ARE RECOMMENDED FOR DISPLAY

4. STANDARD LOGIC INTERMODULAR LINKS

   STANDARD LOGIC INTERMODULAR LINKS ARE SHOWN SORTED BY SOURCE ON DRAWINGS FS00–1–3.1 AND 3.2, SHOWN SORTED BY DESTINATION ON DRAWINGS FS00–1–4.1 AND 4.2, AND SHOWN SORTED BY BUS NAME ON DRAWINGS FS00–1–5.1 AND 5.2

5. SPECIAL LOGIC MODULES

   a) STANDARD LOGIC MODULES SHALL BE USED WHENEVER THE REQUIRED FUNCTIONALITY IS AVAILABLE WITHIN A STANDARD MODULE

   b) NO INTERPOSING LOGIC IS TO BE PROVIDED BETWEEN MODULES. IF THE REQUIRED FUNCTIONALITY IS NOT AVAILABLE USING THE STANDARD LOGIC MODULES, THE PROJECT DESIGNER SHALL DEVELOP PROJECT SPECIFIC SPECIAL LOGIC MODULES IN ORDER TO SATISFY THE REQUIREMENTS OF A PARTICULAR PROJECT

   c) SPECIAL LOGIC MODULES SHALL HAVE A TOTAL INPUT AND OUTPUT COUNT OF NOT MORE THAN 32

   d) SPECIAL LOGIC MODULES SHALL BE DOCUMENTED IN THE SAME MANNER AS STANDARD LOGIC MODULES AS INDICATED IN THE FS00–2 SERIES OF DRAWINGS

6. DETAIL DESIGN LOGIC DRAWINGS

   6.1 DETAIL DESIGN LOGIC DRAWINGS SHALL CONSIST OF:

   a) COPIES OF THE MODULE INTERNAL LOGIC DIAGRAMS FOR THE CURRENT REVISIONS OF THE STANDARD LOGIC MODULES USED WHICH:
      i) SPECIFY THE DRAWING NUMBER AND REVISION IDENTIFIER OF EACH FS00 SOURCE DRAWING
      ii) HAVE BEEN ALLOCATED PROJECT SPECIFIC DETAIL DESIGN LOGIC BUNDLE DRAWING NUMBERS, AND
      iii) HAVE BEEN ENHANCED TO SHOW THE I/O BUSES USED

   b) DIAGRAMS SHOWING THE MODULE INTERNAL LOGIC FOR THE PROJECT SPECIFIC SPECIAL LOGIC MODULES

   6.2 THE LOGIC USED IN PROJECT SPECIFIC LOGIC MODULES BASED ON STANDARD LOGIC MODULES AS PER PARA. 6.1a) ABOVE, SHALL BE:
   a) FOR UNIT STOP/START MODULES, EXACT COPIES OF THE MODULE INTERNAL LOGIC IN THE STANDARD UNIT STOP/START MODULE, NOT ABBREVIATED OR MODIFIED IN ANY WAY EXCEPT FOR PHYSICAL OR EXTERNAL COMMUNICATIONS LINK TERMINATION ALLOCATION
   b) FOR ALL MODULES OTHER THAN UNIT STOP/START MODULES, A COPY OF THE MODULE INTERNAL LOGIC IN THE ASSOCIATED STANDARD LOGIC MODULE EXCEPT LOGIC ASSOCIATED WITH UNUSED STANDARD I/O BUSES MAY BE DELETED. ALTERNATIVELY, THE DETAIL DESIGNER MAY ELECT TO SHOW ALL, OR SOME, OF SUCH UNUSED STANDARD I/O TOGETHER WITH THE ASSOCIATED LOGIC, IN WHICH CASE SUCH I/O SHALL BE LABELLED PNU (i.e. PROGRAMMED BUT NOT USED)

7. PREPARATION AND REVIEW OF DETAIL DESIGN LOGIC DIAGRAMS

   DETAIL DESIGN LOGIC DIAGRAMS AS SPECIFIED IN NOTE 6 SHALL BE PREPARED BY THE CONTRACTOR SUPPLYING THE PUMP CONTROL CUBICLE.
   DETAIL DESIGN LOGIC DIAGRAMS AS SPECIFIED IN NOTE 6 SHALL BE REVIEWED BY THE SENIOR ENGINEER WHO CERTIFIED THE DESIGN SUMMARY LOGIC DRAWINGS. SUCH DRAWINGS SHALL NOT BE ISSUED FOR PROGRAMMING UNTIL CERTIFIED BY THE SENIOR ENGINEER AS BEING IN ACCORDANCE WITH THE DESIGN SUMMARY LOGIC DRAWINGS

8. COMMENCEMENT OF PLC PROGRAMMING

   PLC PROGRAMMING SHALL NOT BE COMMENCED UNTIL ALL OF THE PROJECT SPECIFIC DETAIL DESIGN LOGIC DRAWINGS AS DETAILED IN NOTE 6 HAVE BEEN COMPLETED, CHECKED, REVIEWED AND SIGNED BY THE DESIGNER AND THE REVIEWER

9. PLC PROGRAMMING AND DOCUMENTATION

   PLC PROGRAMMING AND DOCUMENTATION SHALL COMPLY WITH THE REQUIREMENTS OF WATER CORPORATION DESIGN STANDARD DS22 SECTION 14.4 AND WITH THE FOLLOWING REQUIREMENTS:

   a) LOGIC MODULES SHALL BE PROGRAMMED EXACTLY AS SHOWN ON THE CERTIFIED DETAIL DESIGN LOGIC DRAWINGS AND NO ATTEMPT SHALL BE MADE TO OPTIMISE THE LOGIC OR TO OTHERWISE CHANGE THE LOGIC FORMAT

   b) THE CONVENTION SHALL BE ADOPTED THAT LATCH "SETS" OVERRIDE LATCH "RESETS"

   c) EACH PHYSICAL INPUT SHALL CREATE A UNIQUE BUS DESIGNATED IN ACCORDANCE WITH THE DETAIL DESIGN LOGIC DRAWINGS

   d) EACH INPUT FROM AN EXTERNAL COMMUNICATIONS LINK SHALL CREATE A UNIQUE BUS DESIGNATED IN ACCORDANCE WITH THE DETAIL DESIGN LOGIC DRAWINGS

   e) EACH PHYSICAL OUTPUT SHALL BE DRIVEN FROM A SINGLE BUS DESIGNATED IN ACCORDANCE WITH THE DETAIL DESIGN LOGIC DRAWINGS

   f) EACH OUTPUT TO AN EXTERNAL COMMUNICATIONS LINK SHALL BE DRIVEN FROM A SINGLE BUS DESIGNATED IN ACCORDANCE WITH THE DETAIL DESIGN LOGIC DRAWINGS

   g) INPUTS AND OUTPUTS SHOWN ON THE PROJECT SPECIFIC CERTIFIED DETAIL DESIGN LOGIC DRAWINGS AS PNU (PROGRAMMED BUT NOT USED) SHALL BE BROUGHT OUT TO PHYSICAL TERMINALS OR TO AN EXTERNAL COMMUNICATIONS LINK, AS APPROPRIATE

   h) PERMANENT MEMORY LATCHES (e.g. LADDER LOGIC PROGRAMME RETENTIVE COILS) ARE SHOWN IN THESE DRAWINGS AS:

   PERMANENT MEMORY LATCHES SHALL NOT BE USED FOR CONTROL FUNCTIONS UNLESS APPROVED BY THE PRINCIPAL ENGINEER

   i) LOGIC LATCHES WHICH ARE NOT SHOWN IN THESE DRAWINGS AS PERMANENT MEMORY LATCHES SHALL NOT BE PROGRAMMED AS PERMANENT MEMORY LATCHES

   j) ALL INPUT BUSES SHALL BE SHOWN ON THE LEFT HAND SIDE OF THE LOGIC DIAGRAM. ALL OUTPUT BUSES SHALL BE SHOWN ON THE RIGHT HAND SIDE OF THE LOGIC DIAGRAM, WHETHER CREATED USING LOGIC FUNCTIONS OR DERIVED DIRECTLY FROM PLC INPUTS

10. AS CONSTRUCTED LOGIC DIAGRAMS

   FOLLOWING COMMISSIONING OF THE PROJECT, THE PROJECT DETAIL DESIGN LOGIC DRAWINGS (INCLUDING THE PROJECT SPECIFIC LOGIC DIAGRAMS FOR THE STANDARD LOGIC MODULES USED) SHALL BE REVISED TO SHOW THE PLC ADDRESS OF EACH LOGIC BUS AND LOGIC FUNCTION

STANDARD I/O BLOCKS LIST

FS00–2–1.1	STATION STATUS MODULE – PART 1
FS00–2–1.2	STATION STATUS MODULE – PART 2
FS00–2–2	STATION INHIBIT MODULE
FS00–2–3.1	UNIT STOP/START MODULE – PART 1
FS00–2–3.2	UNIT STOP/START MODULE – PART 2
FS00–2–4.1	UNIT STATUS MODULE – PART 1
FS00–2–4.2	UNIT STATUS MODULE – PART 2
FS00–2–5.1	UNIT ELECTRICAL AND HYDRAULIC FAULT MODULE – PART 1
FS00–2–5.2	UNIT ELECTRICAL AND HYDRAULIC FAULT MODULE – PART 2
FS00–2–6.1	UNIT BEARING FAULT MODULE – PART 1
FS00–2–6.2	UNIT BEARING FAULT MODULE – PART 2
FS00–2–7	UNIT AUXILIARIES MODULE
FS00–2–8.1	SURGE VESSEL MODULE – PART 1
FS00–2–8.2	SURGE VESSEL MODULE – PART 2
FS00–2–9.1	TRANSFORMER MODULE – PART 1
FS00–2–9.2	TRANSFORMER MODULE – PART 2
FS00–2–10	STATION ANALOGUES AND TOTALISERS MODULE
FS00–2–11	UNIT ANALOGUES AND TOTALISERS MODULE
FS00–2–12	UNIT VIBRATION MODULE
FS00–2–13	UNIT * BORE STATUS MODULE
FS00–2–14	BORE ANALOGUE MODULE
FS00–2–15.1	SINGLE DUTY MODULE – PART 1
FS00–2–15.2	SINGLE DUTY MODULE – PART 2
FS00–2–16	ABB VSC ACS1000 STOP/START MODULE
FS00–2–17	ABB VSC ACS1000 I/O CONNECTIONS

ISSUE	DATE	GRID	REVISION	DRN	REC	APPD
F	10/2010		"STANDARD LOGIC SYSTEM – DIRECTIONS FOR USE" REVISED; FS00–2–13 TO 17 ADDED TO STANDARD I/O BLOCKS LIST			
E	02/2004		8j) ADDED	TJT	RP	NHJ
D	12/2003		DIRECTION 8g) REVISED; 8b) ADDED	TJT	RP	NHJ
C	11/2002		DIRECTIONS FOR USE REVISED	TJT	RP	NHJ
B	10/2001		NOTE 10 REVISED	AA	RP	NHJ

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DESIGN SURVEY NONE | VERTICAL DATUM NONE | COORDINATE SYS NONE | ASCON SURVEY NONE | DES REF | DES CALC | DES CHD KOG | DRN TJT | Q.C. CHD HdeV | NORTH POINT

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RECOMMENDED 21/08/2001 R PRITCHARD (SIGNED) PRINCIPAL RGP ENG
RECOMMENDED 24/08/2001 N H JOHNSON (SIGNED) SUPERVISING ELECT. ENGINEER, IDB
APPROVED 24/08/2001 A KLITA (SIGNED) PRINCIPAL ENGINEER, IDB

WATER CORPORATION

ELECTRICAL STANDARD DRAWING
MAJOR PUMP STATION
STANDARD LOGIC SYSTEM
DIRECTIONS FOR USE AND STANDARD I/O BLOCKS LIST

FILE | PLAN | CAD | ISSUE F | PROJECT | FS00–1–2 | ORIGINAL SHEET SIZE A1 | MF 31 MAR 2011

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